

Appl. No. 09/955,424

Reply to Examiner's Action dated 01/23/2006

**REMARKS/ARGUMENTS**

The Applicants originally submitted Claims 1-33 in the application. Previously, the Applicants amended Claims 1, 4-5, 9, 12, 15-16, 20, 23, 26-27 and 31 and added Claims 34-36. In the present response, the Applicants have not amended, added or canceled any claims.

The Examiner has indicated that dependent Claims 9, 20 and 31 include allowable subject matter. As argued below, the Applicants believe that each pending claim is allowable. Accordingly, Claims 1-7, 9-18, 20-29 and 31-36 are currently pending in the application.

**I. Rejection of Claims 1-3, 10, 12-14, 21, 23-25 and 32 under 35 U.S.C. §103**

The Examiner has rejected Claims 1-3, 10, 12-14, 21, 23-25 and 32 under 35 U.S.C. §103(a) as being unpatentable over of U.S. Patent No. 6,552,619 to Shastri in view of U.S. Patent 6,018,547 to Arkhipkin, *et al.*, and in further view of U.S. Patent 5,651,031 to Ishizu. The Applicants respectfully disagree.

As recognized by the Examiner, Shastri does not teach or suggest a multi-channel serdes receiver with each receiver including integrators and latches configured to perform demultiplexing of a data signal received thereby as recited in independent Claims 1, 12 and 23. To cure this deficiency, the Examiner cites Arkhipkin. (*See Examiner's Action*, pages 2-3.) Arkhipkin relates to broadband communication systems including systems for transmission and reception of pseudorandom noise sequences (PNSs) and spread spectrum signals. (*See column 1, lines 8-11.*) Arkhipkin discloses a PNS demodulator 264 that includes accumulators, switches and delays. (*See column 2, lines 52-60 and Figures 2B and 2C.*) The accumulators of the PNS demodulator 264, however, are not

Appl. No. 09/955,424  
Reply to Examiner's Action dated 01/23/2006

integrators as asserted by the Examiner. (See Examiner's Final Rejection, page 3.) Instead, the accumulators accumulate the products of subchannels and PNS multipliers for one PNS period as illustrated by the switches and delay elements of Figure 2C. (See column 2, lines 52-60.) The Applicants can find no teaching or suggestion in Arkhipkin of the accumulators performing as integrators.

Additionally, even if the accumulators of the PNS demodulator 264 were integrators, the accumulators are not configured to perform demultiplexing of a serial input signal. Instead, the accumulators are used for demodulating an input signal. (See column 2, lines 52-67 and Figure 2C.) More specifically, one input channel (*i.e.*, I channel or Q channel) is demodulated resulting in one output channel (*i.e.*, I channel out or Q channel out) in Figure 2C. The input channels are not demultiplexed (*i.e.*, deserialized). Thus, Arkhipkin does not teach or suggest integrators and latches configured to perform demultiplexing of a data signal received thereby as recited in independent Claims 1, 12 and 23.

Ishizu has not been cited to cure the above deficiency of Shastri and Arkhipkin. Additionally, the Applicants do not find where Ishizu cures the above deficiency of Shastri and Arkhipkin. Ishizu discloses using integrators in a clock phase detector of the clock recovery circuits (see column 1, line 47 to column 2, line 10 and Figure 26), but does not teach or suggest employing integrators for demultiplexing a data signal. Thus, Ishizu does not teach or suggest integrators and latches configured to perform demultiplexing of a data signal received by a multi-channel serdes receiver as recited in independent Claims 1, 12 and 23.

Appl. No. 09/955,424  
Reply to Examiner's Action dated 01/23/2006

The cited combination, therefore, of Shastri, Arkhipkin and Ishizu does not teach or suggest each of a plurality of channel-specific receivers configured to receive a data signal and include integrators and latches configured to perform demultiplexing of the data signal as recited in independent Claims 1, 12 and 23. As such, the cited combination does not provide a *prima facie* case of obviousness of independent Claims 1, 12 and 23 and Claims dependent thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of independent Claims 1, 12 and 23 and Claims dependent thereon and allow issuance of Claims 1-3, 10, 12-14, 21, 23-25 and 32.

Furthermore, regarding Shastri and Arkhipkin, one skilled in the art would not be motivated to combine the teachings of Arkhipkin with the teachings of Shastri. On the contrary, Shastri is concerned with multi-channel clock recovery circuits (*see* Shastri, column 2, lines 55-58), while Arkhipkin is directed to increasing the spectral efficiency of a spread spectrum system by decreasing the bit rate of an information signal provided to a PNS modulator and by using two PN sequences on both the I and Q channels (*see* column 3, lines 29-33). Arkhipkin and Shastri, therefore, are directed to different problems such that one looking at Shastri would not be motivated to look to Arkhipkin and vice versa. Thus, in addition to failing to teach or suggest all the claim limitations of independent Claims 1, 12 and 23, one skilled in the art would not be motivated to combine the cited references Shastri and Arkhipkin.

Appl. No. 09/955,424

Reply to Examiner's Action dated 01/23/2006

**II. Rejection of Claims 4-7, 11, 15-22, 26-29 and 33 under 35 U.S.C. §103**

The Examiner has rejected dependent Claims 4-7, 11, 15-22, 26-29 and 33 under 35 U.S.C. §103(a) as being unpatentable over Shastri in view of Arkhipkin, Ishizu and in further view of other references. The other references have not been cited to teach or suggest a plurality of channel-specific receivers configured to receive a data signal and include integrators and latches configured to perform demultiplexing of the data signal as recited in independent Claims 1, 12 and 23. Instead, these references have been cited to teach the subject matter of specific dependent claims listed above. Accordingly, the cited combination of Shastri, Arkhipkin and Ishizu with any of the other references does not teach or suggest each and every element of independent Claims 1, 12 and 23. As such, the cited combinations do not provide a *prima facie* case of obviousness of Claims 1, 12 and 23 and Claims dependent thereon. The cited combinations, therefore, do not render dependent Claims 4-7, 11, 15-22, 26-29 and 33 unpatentable and the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of dependent Claims 4-7, 11, 15-22, 26-29 and 33 and allow issuance thereof.

Appl. No. 09/955,424

Reply to Examiner's Action dated 01/23/2006


**III. Conclusion**

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-7, 9-18, 20-29 and 31-36.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC

  
Joel Justiss  
Registration No. 48,981Dated: March 22, 2006

P.O. Box 832570  
Richardson, Texas 75083  
(972) 480-8800